II. AMENDMENTS TO THE SPECIFICATION

Please accept amendments to the specification as follows:

page 4, second paragraph (lines 7-12):

It is an object of the invention ~~to provide a different method for tracking multi-path components of a signal transmitted in a fading environment. It is another object of the invention~~ to provide a rake receiver comprising rake fingers performing low computational early- late detection to track multi-path components of a signal transmitted in a fading environment.

Page 4, third paragraph (page 4, lines 13 - page 5, line 3):

To this end, a method of the invention comprises:

determining a first value representative of an energy of the signal at a first instant before a presumed occurrence of a local optimum of the energy of the signal;

determining a second value representative of the energy at a second instant after the presumed occurrence of the local optimum;

calculating a first product of a first positive integer and the first value and calculating a second product of a

second positive integer and the second value, with the first positive integer smaller than the second positive integer;

generating a first logical value from a comparison between the first and the second products;

calculating a third product from a third positive integer and the first value and calculating a fourth product from a fourth positive integer and the second value, with the third positive integer smaller than the fourth positive integer;

generating a second logical value from a comparison between the third and the fourth products; and,

generating a detector output signal from a difference between the first logical value and the second logical value.

Page 7, first full paragraph (lines 11-22):

Fig.3 is another block diagram of the receiver R300. The receiver R300 comprises the demodulation circuit 305 for extracting the in--phase and quadrature components I and Q further transmitted as a complex signal S* to the rake receiver 400. The rake receiver 400 comprises three rake fingers 410, 412, 414. Each finger ~~410-414~~ 410, 412, and 414 is assigned a multi-path component S1, S2 and S3, respectively, of the received signal S for acquisition and tracking. The rake receiver 400 also comprises a maximal ratio combiner 420 for combining the multi-path components S1-S3

resolved by the fingers ~~410-414~~ 410, 412, and 414 to provide diversity. The resulting signal is the signal R.

Page 7, second full paragraph (lines 23-31):

Fig.4 is a circuit block diagram representing one example of a structure of the rake finger ~~410-414~~ 410, 412, and 414 of the invention. Initially the rake finger ~~410-414~~ 410, 412, and 414 adopts an acquisition mode. Acquisition is performed in the acquisition unit 422 for synchronizing a replica of the code sequence, originally used to spread the information signal, with the multi-path component S1-S3 assigned to the finger ~~410-414~~ 410, 412, and 414. The replica of the code sequence is generated in a pseudo-noise generator 424.

Page 8, first paragraph (lines 1-10):

Thereafter, in a tracking mode, the rake finger ~~410-414~~ 410, 412, and 414 maintains the generated code sequence aligned to the assigned multi-path component S1-S3. The base-band signals I and Q are provided as the complex input signal S* to the rake finger ~~410-414~~ 410, 412, and 414. The signal S* is then branched in two branches for determining early and late components E and L representing respective early and late reception of the assigned signal component S1-S3 with respect to a presumed reception of the signal S1-S3 which is

represented by a peak of the energy of the assigned signal S1-S3.

Page 8, second paragraph (lines 11-23):

In a first branch, the early component E is determined by correlating in a mixer 428 the signal S* with the code sequence taken at a first instant tE (see FIG. 6) before the presumed peak of the energy of the signal S1-S3. The early component E is then determined by processing the output signal of the mixer 428 in a low-pass filter 432 and by complex magnitude squaring in a squared arrangement 436. As shown in Fig.6, a presumed peak of the energy of the assigned signal S1-S3, represented in dashed line, is expected to occur at instant t0. The component E is representative of the energy of the signal S1-S3 taken at the first instant tE before the presumed occurrence at tO of the optimum of the energy of the signal S1-S3.

Page 9, first full paragraph (lines 3-14):

The early and late components E and L are then inputted to a delay detector 500 that processes the two components E and L and determines the early-late state of the reception of the assigned multi-path component S1-S3 indicated by an early-

late signal V. In this embodiment the delay detector 500 is a digital signal processing (DSP) unit. The signal V is then provided to a loop filter 438 where an appropriate correction signal CORR is derived and transmitted to the pseudo-noise generator 424. The correction signal CORR allows monitoring the phase of the code sequence so that the code sequence is kept synchronized with the assigned component S1-S3.

Page 9, last paragraph (lines 20-31):

A detailed embodiment of the detector 500 is given in Fig.5. The detector 500 comprises a calculating unit 510, a calculating unit 530 and a logical comparator 550 for providing a logical signal V1. The signal V1 is obtained from a comparison of a first product K1*E of the early value E and ~~an~~ a positive integer K1 derived in the unit 510 with a second product K2*L of the late value L and ~~an~~ a positive integer K2 derived in the unit 530. In this embodiment K1 is smaller than K2 (K2/K1>1). V1 is 1 when K2*L>K1*E is true as shown in Table 1, V1 is 0 otherwise. V1=0 indicates that E/L>K2/K1>1, i.e. the tracking of the assigned component S1-S3 is early.

Page 10, first paragraph (lines 1-11):

The detector 500 further comprises a calculating unit 520, a calculating unit 540 and a logical comparator 560 for

providing a logical signal V2. The signal V2 is obtained from a comparison of a first product K3*E of the early value E and ~~an~~ a positive integer K3 derived in the unit 520 with a second product K4*L of the late value L and ~~an~~ a positive integer K4 derived in the unit 540. In this embodiment K3 is smaller than K4 (K3/K4<1) . V2 is 1 when K4*E>K3*L is true as shown in Table 1, V2 is 0 otherwise. V2=0 indicates that E/L<K3/K4<1, i.e. the tracking of the assigned component S1-S3 is late.

Page 10, second paragraph (lines 12-15):

The units ~~510-540~~ 510, 520, 530, and 540 may be implemented as logic gates in the form of ICs or alternatively the functions carried out by the units ~~510-540~~ 510, 520, 530, and 540 may be fulfilled by means of instructions in a software component.

Page 10, last paragraph (page 10, line 26 - page 11, line 8):

K1, K2, K3 and K4 may be arbitrarily chosen with K1<K2 and K3<K4. K1 and K3 may be chosen such that K1=K3 and K2 and K4 may be chosen such that K2=K4. For example, K1=K3=2 and K2=K4=3 allow a simple implementation of the units ~~410-440~~ 510, 520, 530, and 540 using a limited number of logic gates. The positive integers K1, K2, K3 and K4 may be fixed to

different constants depending on the sensitivity required for the early-late detection. The values for K1=K3 and K2=K4 may be chosen greater to reduce the on-time zone and to permit sensitive phase control of the code sequence generator 424.